Abstract of the Disclosure

The proposed fast single precision floating point accumulator of the present invention uses base 32 computation in an attempt to completely remove the need for a costly 8-bit subtractor in the exponent path as is commonly found in conventional designs. It also replaces the expensive variable shifter in the mantissa path with a constant shifter which significantly reduces the cost of the present invention relative to earlier floating point accumulators. The variable shifter required for base 2 to base 32 conversion has been moved outside the accumulator loop. This approach allows comparison of the two input exponents using a comparator. The mantissas are shifted by constant amount to bring them into partial alignment. They are then added or the appropriate mantissa is chosen as the result. The input stream to the accumulator does not need to be cumulative.